What is claimed is:

1. Processor, comprising:

a first calculating unit having a data input and an instruction input;

a second calculating unit having a data input and an instruction input; and

a controllable complementation means, which is connected to the data input of the second calculating unit on the output side, for receiving data and for outputting the received data in a switched-off state and for outputting the complement of the received data in a switched-on state; and

a control means for controlling the two calculating units and such that they operate selectively in a high security mode of operation processing complementary data or in a parallel mode of operation processing independent data,

wherein the control means is formed to

put the complementation means in the high-security mode of operation to the switched-on state and to supply the same data to the data input of the first calculating unit and the complementation means, and the same instructions to the instruction input of the first calculating unit and the instruction input of the second calculating unit, such that the first and the second calculating unit process complementary data synchronously, and

put the complementation means in the parallel mode of operation to the switched-off state and supply first data to the data input of the first calculating unit and second data being independent of the first data to the data input of the second calculating unit, and

wherein the control means is further formed to set the high-security mode of operation for security-relevant program parts or programs, and to set the parallel mode of operation for comparatively less security-relevant program parts or programs.

2. Processor, comprising:

a first calculating unit having a data input and an instruction input;

a second calculating unit having a data input and an instruction input; and

a controllable complementation means, which is connected to the data input of the second calculating unit on the output side, for receiving data and for outputting the received data in a switched-off state and for outputting a complement of the received data in a switched-on state; and

a control means for controlling the two calculating units and such that they operate selectively in a high-security mode of operation processing complementary data or are in a power-saving mode of operation, wherein one of the calculating units is switched off,

wherein the control means is formed to

put the complementation means in the high-security mode of operation to the switched-on state and to supply the same data to the data input of the first calculating unit and the complementation means, and the same instructions to the instruction input of the first calculating unit and the instruction input of the second calculating unit, such that the first and the second calculating unit process complementary data synchronously, and

put the second calculating unit in the power-saving mode of operation in the switched-off state,

wherein the control means is further formed to set the high security mode of operation for security-relevant program parts or programs, and to set the power-saving mode of operation for less security-relevant program parts or programs.

3. Processor, comprising:

a first calculating unit having a data input and an instruction input;

a second calculating unit having a data input and an instruction input; and

a controllable complementation means, which is connected to the data input of the second calculating unit on the output side, for receiving data and for outputting the received data in a switched-off state and for outputting a complement of the received data in a switched-on state; and

a control means for controlling the two calculating units and such that they operate selectively in a high-security mode of operation processing complementary data or in security mode of operation processing the same data,

wherein the control means is formed to

put the complementation means in the high-security mode of operation to the switched-on state and to supply the same data to the data input of the first calculating unit and the complementation means, and the same instructions to the instruction input of the first calculating unit and the instruction input of the second calculating unit, such that the first and

the second calculating unit process complementary data synchronously, and

put the complementation means in the security mode of operation in a switched-off state and supply the same data to the data input of the first calculating unit and to the data input of the second calculating unit, and to supply the same instructions to the instruction input of the first calculating unit and to the instruction input of the second calculating unit, and

wherein further a compare means is provided, which is formed to check an output of the first calculating unit and an output of the second calculating unit for consistency and to trigger a preset reaction in dependency thereon.

4. Processor according to claim 1, further comprising:

a third calculating unit; and

a fourth calculating unit;

wherein the third calculating unit and the fourth calculating unit can be controlled by the control means such that they operate selectively in a high-security mode of operation processing complementary data or in a parallel mode of operation processing independent data.

5. Processor according to claim 1, further comprising:

a third calculating unit; and

a fourth calculating unit;

wherein the third calculating unit and the fourth calculating unit can be controlled by the control means such that they operate selectively in a high-security mode of operation processing complementary data or are in a

power-saving mode of operation, wherein the third and/or the fourth calculating unit is switched off.

6. Processor according to claim 1, further comprising:

a third calculating unit; and

a fourth calculating unit;

wherein the third calculating unit and the fourth calculating unit can be controlled by the control means such that they operate selectively in a high security mode of operation processing complementary data or in security mode of operation processing the same data.

7. Processor according to claim 1, wherein the first calculating unit and the second calculating unit are disposed spatially adjacent or intertwined with each other.

8. Processor according to claim 1, wherein the processor is a cryptography or security processor.

9. Processor according to claim 1, wherein the control means is formed to switch dynamically between different modes of operation during operation of the processor.

10. Chip card with a processor according to claim 1.